WHAT IS CLAIMED IS:

1. A method for coding a sequence of data bytes, in which two bits of a data byte form a double bit, and in which each double bit is represented by a time slot frame that has at least four time slots which can assume an on or off value,

wherein the coding in a time slot frame comprises preloading at least one time slot with an off-value at a specified position; and

wherein the time slots that have not been preloaded have, at most, one time slot with an on-value in order to form a logic value of the double bit.

2. The method as claimed in claim 1,

wherein a protection frame follows the time slot frame of the data byte;

wherein the protection frame has a number of time slots that corresponds to previous time slot frames;

wherein at least one time slot in the protection frame is preloaded with the off-value at the specified position in the time slot frames; and

wherein coding in the protection frame is carried out such that a first on-value number from the time slot frames of the data byte is coded with, at most, two non-successive on-values in those time slots of the protection frame that have not been preloaded.

3. The method as claimed in claim 2, in which the time slots of the protection frame are loaded such that a deviation of all the on-value sum values in the time slot frame of the data byte and in the protection frame is at a minimum.

4. The method as claimed in claim 1, wherein the specified position of the preloaded time slot is located at the start or end of the time slot or protection frame.

5. The method as claimed in claim 1, wherein a time slot with an on-value is formed by a pulse sequence.

6. The method as claimed in claim 5, wherein the pulse sequence has an even number of pulses and pauses with a same duty ratio.

7. The method as claimed in claim 6, wherein a pulse has a predetermined number of carrier oscillations.

8. A mobile data memory for non-contacting interchange of a sequence of data bytes with a reader/writer, the mobile data memory comprising a first coding device configured to code a sequence of data bytes, in which two bits of a data byte form a double bit, and in which each double bit is represented by a time slot frame that has at least four time slots which can assume an on or off value,

wherein the coding in a time slot frame comprises preloading at least one time slot with an off-value at a specified position; and

wherein the time slots that have not been preloaded have, at most, one time slot with an on-value in order to form a logic value of the double bit.

9. The mobile data memory as claimed in claim 8, wherein, upon receiving two successive time slots with an on-value, the first coding device is configured to load the specified position of a time slot with an on-value.

10. The mobile data memory as claimed in claim 8,

wherein the first coding device is configured to determine a second number of on-values from the time slot frames in the data byte;

wherein the first coding device is configured to compare the second number of on-values with a first number of on-values that was previously coded in a protection frame; and

wherein, if the first number differs from the second number, the first coding device is configured to load an on-value at the specified position of a time slot in the protection frame.

11. The mobile data memory as claimed in claim 8, further comprising a checking unit configured to interrupt the non-contacting interchange of the sequence of the data bytes upon identification of an on-value at the specified position in a preloaded time slot.

12. The mobile data memory as claimed in claim 11, wherein, after an interruption, the mobile data memory is configured to restart the non-contacting interchange, at least beginning from that part of the sequence of the data bytes that had not been interchanged.

13. A reader/writer for non-contacting interchange of a sequence of data bytes with at least one mobile data memory, the reader/writer comprising a second coding device configured to code a sequence of data bytes, in which two bits of a data byte form a double bit, and in which each double bit is represented by a time slot frame that has at least four time slots which can assume an on or off value,

wherein the coding in a time slot frame comprises preloading at least one time slot with an off-value at a specified position; and

wherein the time slots that have not been preloaded have, at most, one time slot with an on-value in order to form a logic value of the double bit.

14. The reader/writer as claimed in claim 13, wherein, upon receiving two successive time slots with an on-value, the second coding device is configured to load the specified position of a time slot with an on-value.

15. The reader/writer as claimed in claim 13,

wherein the second coding device is configured to determine a third number of on-values number from the time slot frames in the data byte;

wherein the second coding device is configured to compare the third number of on-values with a first number on values that was previously coded in a protection frame; and

wherein, if the first number differs from the third number, the second coding device is configured to load an on-value at the specified position of a time slot in the protection frame.

16. The reader/writer as claimed in claim 13, further comprising a checking unit configured to interrupt the non-contacting interchange of the sequence of the data bytes upon identification of an on-value at the specified position in a preloaded time slot.

17. The reader/writer as claimed in claim 16, wherein, after an interruption, the reader/writer is configured to restart the non-contacting interchange, at least beginning from that part of the sequence of the data bytes that had not been interchanged.

18. An identification system, comprising:

at least one mobile data memory; and

a reader/writer;

wherein the mobile data memory and the reader/writer interchange sequences of data via a non-contacting data transmission path;

wherein at least one of the mobile data memory and the read/writer comprises a coding device configured to code a sequence of data bytes, in which two bits of a data byte form a double bit, and in which each double bit is represented by a time slot frame that has at least four time slots which can assume an on or off value;

wherein the coding in a time slot frame comprises preloading at least one time slot with an off-value at a specified position; and

wherein the time slots that have not been preloaded have, at most, one time slot with an on-value in order to form a logic value of the double bit.

19. The identification system as claimed in claim 18, wherein the identification system is configured to operate in an ISM frequency band on the basis of the ISO/IEC 1443 standard.

20. The identification system as claimed in claim 18, wherein the identification system is configured to operate in an ISM frequency band on the basis of the ISO/IEC 15693 standard.

21. The identification system as claimed in claim 19, wherein the ISM frequency band comprises a 13.56 MHz frequency band.

22. The identification system as claimed in claim 20, wherein the ISM frequency band comprises a 13.56 MHz frequency band.